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Amendments to the Drawings:

Included in the amendment are an "Annotated Sheet Showing Changes" and a "Replacement Sheet" for Figs. 4C, 8, and 9.

In Fig. 4C the equations in Syntax/Operation block 460 have been modified to correspond with the specification and to correct three typos. Two of the typos concern a parenthesis inadvertently included in an equation and the third typo concerns the labeling of the 16th instruction. The equation:

 $(V[01]+VIMOFFS) + 1)[UnitVIM] \leftarrow 2^{nd}$ Instruction following LV2

and

(V[01]+VIMOFFS) + InstrCnt)[UnitVIM]←(InstrCnt)th Instruction following LV2

have been amended to:

(V[01]+VIMOFFS) + 1)[UnitVIM]← 2nd Instruction following LV2

and

 $(V[01]+VIMOFFS) + InstrCnt)[UnitVIM] \leftarrow (InstrCnt+1)^{th}$ Instruction following LV2

to correctly correspond to the text immediately below the last equation which correctly states:

"InstrCnt is a binary coded number, 0 thru F, that represents from 1 to 16 instructions that can be

loaded into up to 16 consecutive UnitVIM locations." For example, for the 16th instruction to be

loaded, InstrCnt would be set to a maximum setting of F, a binary setting of all 1's in the four bit

InstrCnt bit field of bits 18-21 in LV2 instruction 450 Fig. 4C, and the equation would then

indicate, by substituting F for InstrCnt, as follows:

(V[01]+VIMOFFS + F)[UnitVIM]←(F + 1)th Instruction following LV2

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which equivalently in decimal is:

(V[01]+VIMOFFS + 15)[UnitVIM]←(16)th Instruction following LV2

Consequently, with (V[01]+VIMOFFS)=b as the start address where the first instruction is loaded, sixteen VIM addresses b to b+15 are loaded, where b+15 is the 16th instruction loaded.

In Fig. 8, high address label A-1 on the ALU VIM 903 is amended to C-1 and high address label B-1 on the adjacent MAU VIM is amended to D-1 to be consistent with partitioned VIM section high address labels of Fig. 6 ALU instruction VIM 624 and MAU instruction VIM 626, respectively. The capacities of the separate VIM sections are indicated by the 0-(A-1) store VIM 620, 0-(B-1) load VIM 622, 0-(C-1) ALU VIM 624, 0-(D-1) MAU VIM 626, and 0-(E-1) DSU VIM 628. Each separate VIM section as shown in Figs. 6 and 8 may have a different capacity depending upon application and implementation requirements.

In Fig. 9, high address label B-1 on the ALU VIM 903 is amended to C-1 to be consistent with partitioned VIM section high address labels of Fig. 6 ALU instruction VIM 624 and newly amended Fig. 8 ALU VIM 903. In addition, circular label d 937 is amended to c 937 to be consistent with the similar label in Fig. 8 associated with the VIM ALU 903.

Annotated Sheet Showing Changes

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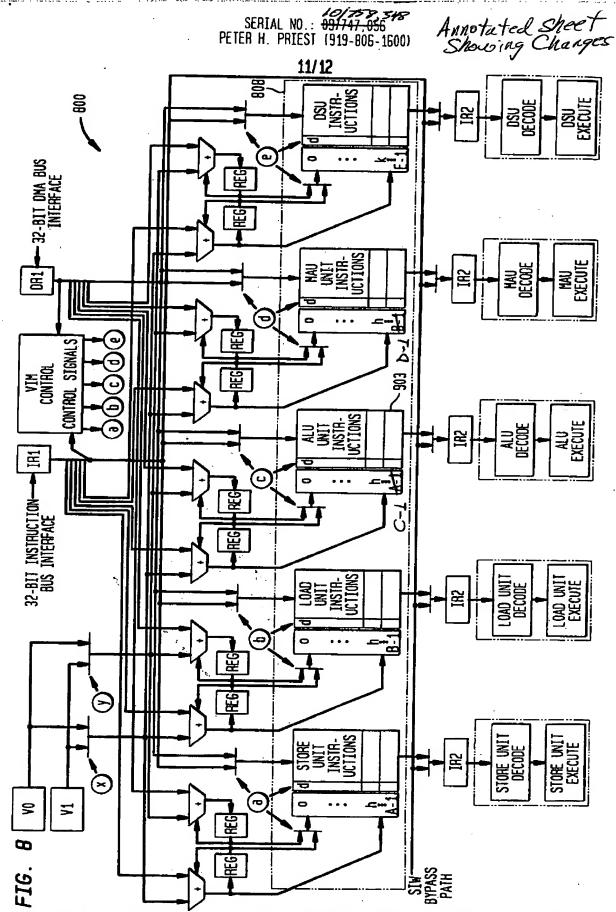
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	FIG. 4C	
LV2- LOAD/HODIFY VLIW-	IFY VLIW- 2 — 455	450
		•
31 30 29 Grain S/P	25 24 23 22 21 20 19 18 1	16 15 14 13 12 11
100 000	ומה ה דו מ זופנערענ	UnityIM 0 0 0 0 0 VimOffs
Syntax/Operation	460 /	
Instruction	Operands	Operation
		if (LI=0) Load disable bit only disable bit @ (V[01]+VIMOFFS)[UnitVIM] - d
		if (LI=1) Load instructions disable bit @ (V[O1]+VIMOFFS)[UnitVIM] d
		Load next Instruct instructions into (V[01]+VINOFFSI[UnitVIN] —— 1st Instruction following LV2
[48].[87]	LI, u-UnitVIN, V(01), VIHOFFS, Instrent, d	(V[O1]+VIMOFFS*+1)[UnitVIM] 2nd Instruction following LV2
		(V[01]+VIMOFFS**InstrCnt}[UnitVIN] — {InstrCnt} th Instruction following LV2 Instruction following LV2 InstrCnt is a binary coded number. 0 thru F. that represents from 1 to 16 instructions that can be loaded into up to 16 consecutive UnitVIN locations

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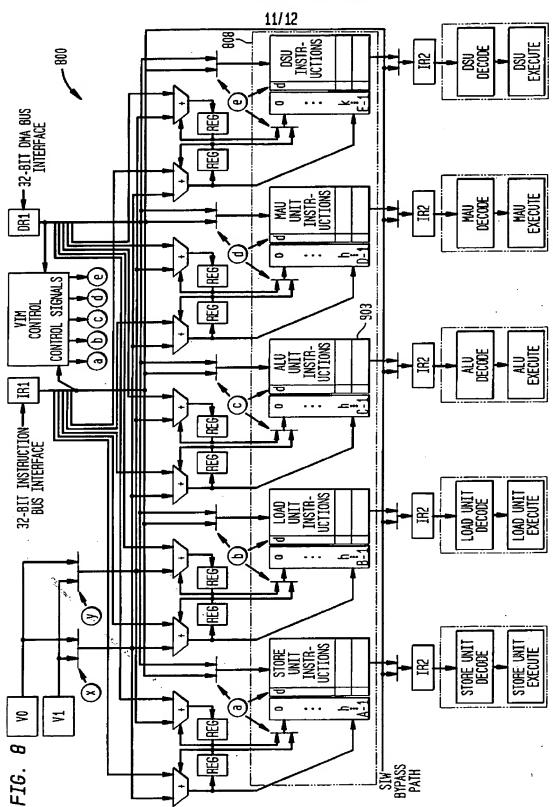
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J	450	7 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 UnitVIM 0 0 0 0 0 Vb 0 VimOffs		Operation	if (LI=0) Load disable bit only disable bit @ (V 01]+VIMOFFS)[UnitVIM] d	if (LI•1) Load instructions disable bit @ (V[01]+VINOFFS)[UnitVIM] d	Load next Instructions into (V[01]+VIMOFFS)[UnitVIM] 1st Instruction following LV2	(V[01]+VIMOFFS+1)[UnitVIM] - 2nd Instruction following LV2	(V[01]+VINOFFS+InstrCnt)[UnitVIN] —— (InstrCnt+1) th Instruction following LV2 InstrCnt is a binary coded number, 0 thru F, that	loaded into up to 16 consecutive UnitVIM locations
FIG. 4C	LV2- LOAD/MODIFY VLTW- 2 — 455 Encoding	29 28 27 26 25 24 23 22 21 20 19 18 1 S/P CtrlOp 0 LI d Instront	peration	Instruction Operands		:		LV2.[SP] LY U=UnitVIM, V[01], VIMOFFS, Instruct, d		



PAGE 26/29 * RCVD AT 9/16/2004 10:54:36 AM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/3 * DNIS:8729306 * CSID:919 806 1690 * DURATION (mm-ss):09-02

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Annotated Sheet Showing Changes 12/12 CONTROL SIGNAL VIM CONTROL 927~ FIG.

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